REMARKS

Amendments

Claims 1-38 are pending. Claim 34 is amended, as requested by the Examiner, to clarify that the BIOS is stored in a non-volatile memory device.

In the Drawings

The Examiner has stated in both the present Final Office Action and in the Office Action mailed on December 27, 2004, that Figure 5 should be designated by a legend such as –Prior Art— "because only what is old is illustrated" and requests that a Replacement Drawing in compliance with 37 CFR 1.121(d), be submitted. The Examiner cited Paragraph [0039] of the Present Application in the objection, which refers to the "older systems such as the system 500 of figure 5." Applicant respectfully traverses this objection and continues to maintain that the system 500 shown in Figure 5 is not prior art for the following reasons.

Applicant notes that Paragraph [0026] of the Brief Description of the Drawings states that "[f]igure 5 details a synchronous memory system containing a BIOS memory device, a synchronous Flash memory of the present invention, and a synchronous RAM." Applicant therefore respectfully maintains that the system 500 of Figure 5 contains "a synchronous Flash memory of the present invention" and that, even though Figure 5 is similar to other existing systems, it is clearly labeled and described as containing an embodiment of the present invention. Furthermore, as provided in Paragraph [0038], "In the system of Figure 5, the non-volatile memory device 508 containing the BIOS code of the system 500, also contains the software routines necessary for the system to access the synchronous Flash memory device 506 and issue the "STOP" command to end its looping initialization cycle." Applicant contends that a looping initialization cycle in accordance with the present invention has not been identified in the prior art. Thus, to label Figure 5 as prior art would be inconsistent with the express description of the figure. Applicant therefore continues to maintain that the system of Figure 5 is not prior art and that this is clearly stated in the description. Applicant also maintains, as before, that the statement cited by the Examiner in Paragraph [0039], "older systems such as the system 500 of

figure 5," is not an admission of prior art but simply a reference to the architecture of this system 500, and not to its components as described.

In response to the Examiner's statement in his "Response to Arguments" section starting on page 8 of the Final Office Action mailed on June 16, 2005, that "[w]ith respect to the applicant's arguments that figure 5 is not admitted prior art, ... at page 5 of the instant remarks, with respect to claim 32 in particular, applicants state that,'...various forms of memory devices and busses, including synchronous and asynchronous memory devices and busses, are well known in the art.' Accordingly the objection has been maintained." Applicant notes that this generalized statement of the art does not overcome the express statement as to the novel functionality of the system 500 as described with reference to Figure 5.

In view of the above arguments, Applicant respectfully requests that the Examiner's objection to Figure 5 be withdrawn because the system illustrated in Figure 5 is expressly described to contain novel elements of the invention and thus is not prior art.

Claim Rejections Under 35 U.S.C. § 102

Claims 1, 4-10, 12-14, 17-20, 22-31, and 33-36 were rejected under 35 U.S.C. § 102(a) as being anticipated by applicants' admitted prior art (the AAPA). Applicant respectfully traverses this rejection and submits that claims 1, 4-10, 12-14, 17-20, 22-31, and 33-36 are allowable for at least the following reasons.

The claims recite limitations to iterating, continuously looping, and repeating initialization cycles. The Office Action has not identified any admission or prior art reference corresponding to such iterating, continuously looping or repeating initialization cycles. A device that initiates an initialization in response to a control signal and executes that initialization once to completion cannot read on Applicant's claim as it is neither iterating, continuously looping or repeating as required in Applicant's claims. Thus, the Office Action fails to identify a reference teaching each and every limitation of Applicant's claims. On this basis alone, Applicant contends that a rejection under 35 U.S.C. § 102(a) cannot be maintained.

In rejecting claims 1, 4-10, 12-14, 17-20, 22-31, and 33-36, the Examiner stated that "[a] synchronous flash memory interface is disclosed in paragraph 7. The synchronous flash memory

device beginning initialization upon receiving a power signal (RP#) on a power bus (signals are inherently delivered on a bus) is disclosed in paragraph 28 and in prior art figure 2. Stopping the initialization in response to an external command is inherent in the prior art figure 2 – a computer must be told what to do. Therefore an "external command" must be issued to stop the initialization."

Applicant respectfully maintains, that even if the Examiner is correct in his assertions of Applicant's Admissions of Prior Art, which the Applicant disputes, the synchronous Flash memory disclosed in Paragraphs [0007], [0028], and Figure 2 does not teach or disclose all elements of the Applicant's claimed invention. Applicant maintains that Paragraphs [0007], [0028] and Figure 2 of the Present Application teach a synchronous Flash memory that starts its initialization cycle only upon receiving an external command, in the form of a RP# signal or a LCR command which is asserted by an external controller after power is up and stabilized, and then completes its initialization 50μS - 100μS later without receiving an external command that terminates the cycle. Applicant therefore submits that Paragraphs [0007], [0028] and Figure 2 of the Present Application do not teach a synchronous Flash memory that starts its initialization cycle upon receiving a power signal and iteratively, continuously or repeatedly executes this initialization cycle until it is terminated by an external command, as claimed by the Applicant.

Applicant's claim 1 recites, in part, "wherein the synchronous Flash memory device begins an iterating initialization cycle upon receiving a power signal on a power bus, and stops the iterating initialization cycle upon receiving an external command." As detailed above, Applicant submits that the AAPA fails to teach or disclose such a synchronous Flash memory device that begins an iterating initialization cycle upon receiving a power signal on a power bus, and stops the iterating initialization cycle upon receiving an external command. As such, the AAPA fails to teach or disclose all elements of independent claim 1.

Applicant's claim 8 recites, in part, "wherein the memory device commences a continuously looping initialization cycle upon receiving a power signal, and stops the continuously looping initialization cycle upon receiving an external signal." As detailed above, Applicant submits that the AAPA fails to teach or disclose such a memory device that begins an iterating initialization cycle upon receiving a power signal, and stops the iterating initialization

cycle upon receiving an external command. As such, the AAPA fails to teach or disclose all elements of independent claim 8.

Applicant's claim 17 recites "[a] method of initializing a synchronous Flash memory device comprising commencing a continuously looping initialization cycle upon receiving a power signal; and stopping the continuously looping initialization cycle upon receiving an external command." As detailed above, Applicant submits that the AAPA fails to teach or disclose such a method. As such, the AAPA fails to teach or disclose all elements of independent claim 17.

Applicant's claim 22 recites "[a] method of initializing a memory device comprising starting a repeating initialization cycle upon receiving a power signal on a power distribution line; and stopping the repeating initialization cycle upon receiving an external command." As detailed above, Applicant submits that the AAPA fails to teach or disclose such a method. As such, the AAPA fails to teach or disclose all elements of independent claim 22.

Applicant's claim 28 recites, in part, a system having a synchronous Flash memory device "wherein the synchronous Flash memory device begins an iterating initialization cycle upon receiving a power signal on a power bus, and stops the iterating initialization cycle upon receiving an external command." As detailed above, Applicant submits that the AAPA fails to teach or disclose such a system having a synchronous Flash memory device that begins an iterating initialization cycle upon receiving a power signal on a power bus, and stops the iterating initialization cycle upon receiving an external command. As such, the AAPA fails to teach or disclose all elements of independent claim 28.

Applicant respectfully contends that claims 1, 17, 22 and 28 have been shown to be patentably distinct from the cited reference. As claims 4-10, 12-14, 18-20, 23-27, 29-31 and 33-36 depend from and further define claims 1, 17, 22 and 28, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(a) and allowance of claims 1, 4-10, 12-14, 17-20, 22-31, and 33-36.

Claims 37-38 were rejected under 35 U.S.C. § 102(e) as being anticipated by Kessler (U.S. Patent No. 6,820,196). Applicant respectfully traverses this rejection and reserves the right to swear behind the cited reference. The Applicant submits that claims 37-38 are allowable for at least the following reasons.

As noted with respect to the rejections under 35 U.S.C. § 102(a), a device that initiates an initialization in response to a control signal and executes that initialization once to completion is not iterative as required in Applicant's claims 37 and 38. Thus, the cited reference fails to teach each and every limitation of Applicant's claims. On this basis alone, Applicant contends that a rejection under 35 U.S.C. § 102(e) cannot be maintained.

Applicant continues to maintain that Kessler teaches a television set-top-box (STB) that checks the contents of and selectively initializes the data contents of an internal Flash memory device upon power up. Applicant has carefully reviewed the reference and has not found reference in Kessler to the internal device initialization that the Flash memory device must perform before it can make itself available on the data bus for read and write access by the processor, as maintained by the Examiner. Applicant respectfully maintains that the cited Figures 1 and 3 of Kessler refer to the system (the STB) powering up, checking the protected/formatted status of the Flash memory, and initializing the Flash memory data contents if the device is not formatted. (*See, e.g.*, Kessler, Abstract, Figures 1 and 3, Column 1, lines 48-63, and Column 3, lines 10-29). Applicant therefore respectfully submits that Kessler does not teach or disclose a synchronous Flash memory that begins to iterate an initialization cycle upon receiving Vcc and stops the initialization cycle in response to an external command.

Applicant's claim 37 recites, in part, a computer system that has "a memory device coupled to the host controller, wherein the memory device begins to iterate an initialization cycle in response to Vcc, and stops iterating the initialization cycle in response to the host controller." As detailed above, Applicant submits that Kessler fails to teach or disclose such a memory device that begins an iterating initialization cycle in response to Vcc, and stops iterating the initialization cycle in response to the host controller. As such, Kessler fails to teach or disclose all elements of independent claim 37.

Applicant's claim 38 recites a method of operating a computer system "coupling a host controller to a memory device; detecting Vcc in the memory device; starting an iterating initialization cycle in the memory device; and stopping iteration of the initialization cycle in the memory device in response to a software command from the host controller." As detailed above, Applicant submits that Kessler fails to teach or disclose such a method. As such, Kessler fails to teach or disclose all elements of independent claim 38.

Applicant respectfully contends that claims 37-38 have been shown to be patentably distinct from the cited reference. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(e) and allowance of claims 37-38.

Claim Rejections Under 35 U.S.C. § 103

Claims 2-3, 11, 21, and 15-16 were rejected under 35 U.S.C. § 103(a) as being anticipated over applicants' admitted prior art in view of SGS-THOMSON ST 10F 166. Applicant respectfully traverses this rejection and feels that claims 2-3, 11, 21, and 15-16 are allowable for the following reasons.

Applicant continues to respectfully note that, as stated above in regards to the rejection of independent claims 1, 8 and 17 from which claims 2-3, 11 and 21 depend, the AAPA fails to teach or disclose such a memory device that begins an iterating initialization cycle upon receiving a power signal, and stops the iterating initialization cycle upon receiving an external command. As such, the AAPA fails to teach or disclose independent claims 1, 8 and 17 and therefore does not teach or suggest all elements of claims 2-3, 11 and 21. In addition, Applicant respectfully maintains that cited reference ST10F166 discloses a microcontroller with an internal 256k Flash memory and thus submits that ST10F166 also does not teach disclose such a memory device that begins an iterating initialization cycle upon receiving a power signal, and stops the iterating initialization cycle upon receiving an external command. Therefore combining the elements of the AAPA with cited reference ST10F166 does not teach or suggest all elements of claims 1, 8 and 17. The Applicant therefore maintains that claims 1, 8 and 17 are thus allowable over the AAPA and cited reference ST10F166, either alone or in combination. As claims 2-3, 11

and 21 depend from and further define claims 1, 8 and 17, claims 2-3, 11 and 21 are also deemed allowable.

In regards to independent claims 15 and 16, the Applicant respectfully submits that, as stated above, the AAPA fails to teach or disclose such a memory device that begins an iterating initialization cycle upon receiving a power signal, and stops the iterating initialization cycle upon receiving an external command. As such, the AAPA fails to teach or suggest all elements of claims 15 and 16. In addition, cited reference ST10F166 also does not teach disclose such a memory device that begins an iterating initialization cycle upon receiving a power signal, and stops the iterating initialization cycle upon receiving an external command. Therefore combining the elements of the AAPA with the cited reference ST10F166 does not teach or suggest all elements of claims 15 and 16. The Applicant therefore maintains that claims 15 and 16 are thus allowable over the AAPA and cited reference ST10F166., either alone or in combination.

Applicant respectfully contends that claims 2-3, 11, 21, and 15-16 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 2-3, 11, 21, and 15-16.

Claims 32 was rejected under 35 U.S.C. § 103(a) as being unpatentable over applicants' admitted prior art. Applicant respectfully traverses this rejection and feels that claim 32 is allowable for the following reasons.

Applicant respectfully notes that, as stated above in regards to the rejection of independent claim 28 from which claim 32 depends, the AAPA fails to teach or disclose such a memory device that begins an iterating initialization cycle upon receiving a power signal, and stops the iterating initialization cycle upon receiving an external command. As such, the AAPA fails to teach or disclose independent claim 28 and therefore does not teach or suggest all elements of claim 32.

CONCLUSION

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

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